Broadband GaN MMICs for Analog Interference Suppression

Paige Danielson and Zoya Popović
The University of Colorado Boulder, Boulder, CO, 80309

Receivers are subject to unwanted signals from both internal and external sources, which can overload the electronics, i.e. the analog to digital converter (ADC). Traditionally, this problem is addressed by using filters, but for broadband systems, these signals are no longer always out-of-band so a different, tuneable solution is needed. One solution is an interferometer topology. This topology, whose block diagram shown in Fig. 1(a), splits the incoming signal into two paths, adjusts the phase and magnitude of the paths, and recombines the paths so they are of the same magnitude and 180° out of phase so there is destructive interference and a spectral notch at a specific frequency. The phase delay is adjusted through the use of an artificial transmission line that used transistors as varactors. The proof of concept was shown in a GaAs MMIC across 6–12 GHz (P. Danielson, et al., "GaAs MMIC Inteferometer for Broadband Interference Suppression," *2022 17th European Microwave Integrated Circuits Conf.*, Milan, Italy). To address the need for better linearity and higher power handling need when higher power unwanted signals are present, a hybrid circuit GaN version across 2–4 GHz with no gain is shown in (M. Robinson, et al., "Linear Broadband Interference Suppression Circuit Based on GaN Monolithic Microwave Integrated Circuits," *IET Circuits, Devices, and Systems*, vol. 17, no. 4, Jul. 2023). This work presents two fully monolithically integrated solutions in WIN Semiconductors' NP15 GaN process that improve on previously published versions by using noise matched amplifiers to achieve low noise figure and GaN for high power handling and linearity.

The first solution, Fig. 1(b), is a two-stage LNA followed by a variable delay artificial transmission line made with transistors in a cold-FET topology which allows for higher levels of capacitance and capacitance variation. This circuit covers 6–12 GHz, with gain over 12 dB and phase variation of over 130° at 9 GHz, the center of the band. External combining circuitry is needed for interferometer function. Simulations show with the external combining, a spectral notch can be placed anywhere across the octave. The second solution, Fig. 1(c), is an integrated interferometer. Each path has a two-stage LNA followed by a variable transmission line that uses source and drain grounded transistors as varactors. This fully integrated version has delay lines in both paths which allows for higher levels of tuning of the notch placement which can easily covering the 6–12 GHz octave while achieving gain over 10 dB at other frequencies. Simulations and measurements of both MMICs will be presented.

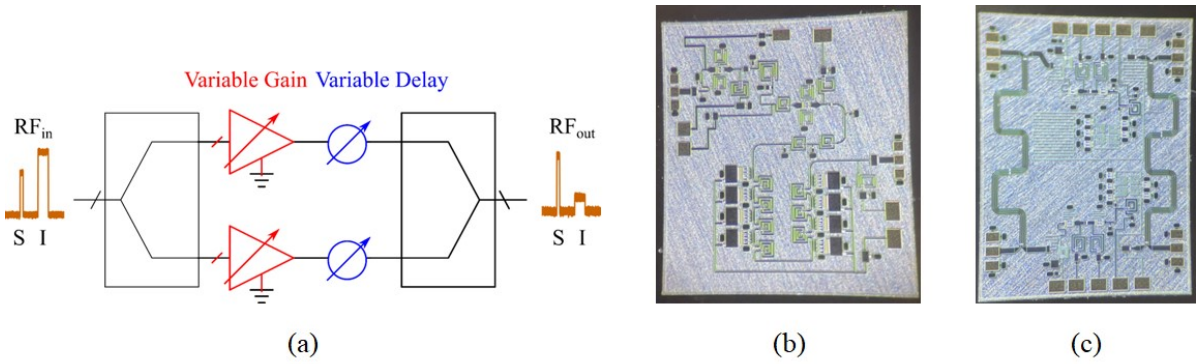

Figure 1: (a) Block diagram of the interferometer topology. Picture of WIN Semiconductors' GaN NP15 chip of a (b) LNA followed by cold-FET transistors delay line and (c) integrated interferometer with LNAs followed by source and drain grounded transistors delay line.