RFSoC-Based Digital Beamformer for Millimeter-Wave MIMO Applications
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Abstract—This paper presents a novel 4-channel digital beamforming receiver architecture for 5G millimeter-Wave cellular communications. The receiver is based on a code-multiplexed topology where all the channels are encoded with unique orthogonal Walsh-Hadamard codes and multiplexed into a single-channel. A single wideband analog-to-digital converter (ADC) on RF-SoC FPGA is employed at the digital back-end which significantly reduces the cost, complexity and power consumption of the hardware realization. The digital signal processor (DSP) algorithms for multi-channel synchronization and beamforming are implemented on the Xilinx ZCU111 RF-SoC FPGA prototyping platform. An end-to-end measurement setup including ultrawideband antenna array (TCDA), a custom-designed and fabricated Encoder Circuit Board (ECB) and FPGA processor are also included for system validation. A maximum clock frequency of 400 MHz was used for generation of the unique codes and decoding the desired signals at the receiver end. To the best of the author’s knowledge a maximum of 36 dB interchannel interference ratio (ICI) was achieved which is the highest to be reported in literature till dates.

I. INTRODUCTION

Millimeter-Wave frequency range is of great research interest since it offers large bandwidth and high data rate. Migrating to wireless technologies like MIMO, 2D communications, beamforming and spatial multiplexing are some of the exciting approaches to increase the system capacity and spectral efficiency [1]. Millimeter-wave frequency band (30-300) GHz is a preferable choice to exploit the higher frequency spectrum and wider bandwidth to deliver an ubiquitous low-latency high data-rate communication link [2]. Hardware realization of mm-Wave systems for beamforming applications comes with several implementation challenges particularly at such high carrier frequencies [3].

Although short wavelengths at mm-Wave frequency are susceptible to large propagation losses, this can be compensated by the array gain since a large number of antenna elements can be realized in a smaller form-factor device. Hence, there is a growing interest in realizing single-chip solution to integrate multiple-antenna system modules for beamforming. Analog beamforming approaches include either true time delay elements or phase-shifters behind each antenna element to constructively adjust the desired beam. Whereas, hybrid digital beamforming or fully-digital beamformers include dedicated ADCs in each of the RF front-end. This significantly increases the cost and power consumption [4]. At mm-Wave frequencies, including dedicated phased-shifters and ADCs for each RF chain may no longer be a practical solution form large number of simultaneous beams in high-capacity systems such as MIMO.

In this paper, a state-of-the-art experimental validation of a 4-channel MIMO receiver architecture is proposed for beamforming applications using orthogonal coding technique. This approach utilizes the code division multiplexing (CDM) technique at the analog front-end. A single FPGA board at the digital baseband is used to encode the baseband signal from each channel as well as decorrelate the original signal. The RF-SoC ZCU111 FPGA evaluation board from Xilinx integrates high-speed analog-to-digital converters (ADCs), digital-to-analog converters (DACs), ARM-based processing unit and FPGA fabric on the same die. Thus, this approach of single high-speed RF-SoC ADC at the digital end significantly reduces the overall power consumption and cost of the system by 78% and 85% respectively [3] and additionally allows beam steering and beamforming at the digital baseband.

II. HARDWARE REALIZATION AND SYSTEM VALIDATION

A. Walsh Hadmard Code Orthogonality

The proposed receiver employs the same set of codes to encode and decode the signals at the receiver respectively. The significance of WH codes is it’s perfect orthogonal properties which is very important when several channels are multiplexed into one. A code length of 16 was used for this work which is generated by the following matrix

$$\begin{bmatrix}
H_N & H_N \\
H_N & H_N
\end{bmatrix}$$

(1)

where \(H_N\) refers to the WH code of length \(N\). The signal at the \(k^{th}\) element after being encoded at the analog end can
only be correctly decoded at the digital baseband only if the codes show the orthogonal properties of
\[
\int_0^{T_d} c_k(t) c_k(t) = 1 \quad (2)
\]
\[
\int_0^{T_d} c_k(t) c_i(t) = 0 \quad (3)
\]
where, \(c_k\) and \(c_i\) are the code sequences in the desired and interfering paths respectively.

**TABLE I**

<table>
<thead>
<tr>
<th>Component</th>
<th>Part Number</th>
<th>Frequency Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiplier Chip</td>
<td>ADL9351 (Analog Device)</td>
<td>0-2 GHz</td>
</tr>
<tr>
<td>RF Transformer</td>
<td>TC1-1-13M+ (Mini Circuits)</td>
<td>4.5-3000 MHz</td>
</tr>
<tr>
<td>Power Combiner</td>
<td>JCP8-10+ (Mini Circuits)</td>
<td>5-1000 MHz</td>
</tr>
</tbody>
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**C. Encoder Circuit and Digital Baseband Processor**

The Walsh-Hadamard (WH) code is generated from Xilinx ZCU111 FPGA board. A digital circuit is designed using MATLAB System Generator where circuit blocks such as binary counter, slices, multiplexers, and logic gates are used. The generated bitstream is synthesized in the FPGA fabric. The ZU28DR chip incorporates 8x12-bit RF-ADCs with a maximum sampling rate of 4.096 GSPS integrated with the ARM processing system (PS) in a single platform. To introduce the WH codes into the downconverted signal chain a custom-designed 6-layer circuit board titled as Encoder Circuit Board (ECB) is fabricated. The objective is to multiply the incoming all four intermediate-frequency (IF) signals with unique code sequence and multiplex all the signals into a single channel. The ECB consists of the components listed in Table 1.

**D. Measurement Results**

Fig.3 shows the decoded signals and achieved ICI depicting the fact that inclusion of WH codes to decode desired channel successfully extracts signal information from multiple antenna elements in a MIMO setup.

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**REFERENCES**