An Ultra-wideband Spectrometer for The Next Generation of the Event Horizon Telescope Project

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The Event Horizon Telescope (EHT) is a very long baseline interferometry (VLBI) array observing blackholes at millimeter and sub-millimeter wavelengths. It achieves an angular resolution of ~ 20 microarcseconds by combining data gathered at radio telescopes on four continents, with a maximum baseline comparable to the diameter of the Earth.

The EHT telescopes are currently equipped to digitize and record an aggregated bandwidth of 16 GHz (4 GHz x 2 sidebands x 2 polarizations). In the standard EHT backend configuration, four Roach2 Field-Programmable-Gate-Array (FPGA) boards digitize the data into 8 streams, re-quantize them, and transfer them to recorders. Future EHT receivers will provide access to at least 32 GHz of bandwidth. A new digitization scheme with wider channel bandwidth is desirable.

In this paper, we describe our work on a new ultra-wideband backend system for EHT project. Current Roach2s are obsolete and cannot be used to process 8 GHz sidebands, hence a new development board is required. Our prototype uses the ZCU111 FPGA board manufactured by Xilinx. This board is equipped with the first generation RFSoc Zynq chips featuring eight analog-to-digital converters (ADCs) that operate at 4 Giga-samples-per-second(Gsps) with 4 GHz of analog bandwidth. To double the Nyquist bandwidth, our design interleaves two ADCs, however, higher bandwidths could be resolved by technology advancement in the future Xilinx RFSoc chips' generations. Interleaving ADCs allows us to process the current 4 GHz receiver IF bandwidths, enabling the full 16 GHz receiving bandwidth of current EHT sites to be processed on a single board. The introduction of an analog IQ mixer ahead of the digitization enables future 8 GHz IF bandwidths to be processed and recorded, after digital sideband separation on the FPGA. The ZCU111 includes an ARM processing systems (PS) and programmable logic (PL) parts; the computationally intensive tasks are implemented on PL side and system controller and data collection jobs are done by a standalone application written by C running on the PS. Monitoring software has also been made to visualize the data and log the performance. We will present our design and show preliminary results.