Low-Power Highly Efficient Voltage-Boosting Rectifier for Wide-band Inductively-Coupled Power Telemetry

Ramaa Saket Suri, Nishat T. Tasneem, Ifana Mahbub
Department of Electrical Engineering
University of North Texas
Denton, TX, USA
ramaasaketsuri@my.unt.edu

***Abstract*— Wireless power transfer has been studied significantly in the past couple of years for implanted biomedical devices. Due to the extreme power constraints, implantable devices need efficient AC-DC power rectification. This paper presents a low-power rectifier for a wideband wireless power transfer system. The 10-stage rectifier is designed using a standard 130 nm BiCMOS process. The proposed design can rectify voltages as low as 100 mV, which is a low voltage that traditional rectifiers are not able to rectify. The rectifier has a wider frequency operation range of 10 kHz – 100 MHz compared to the previous works where the maximum operating frequency is up to 40-50 MHz. The designed rectifier is able to achieve a power conversion efficiency of 51% with 100 mV 7.25 MHz input signal, which make it highly applicable for the wireless power transfer applications for implantable sensors.**

I. INTRODUCTION

The improvement in wireless power transfer efficiency depends on the reliable power supply to the implants. The efficiency of the power transmission system should be optimized while taking care of the footprint of the system and limiting tissue damage due to the excessive power dissipation of the active circuits. The overall power transfer efficiency largely depends on the AC-DC power conversion efficiency performance as it will ensure the required DC power to the implant. The optimal frequency at the receiving end for an inductively coupled near-field operation is around 100 MHz at the ISM band [1]. The required DC power to the implants typically ranges from hundreds of µW to a few mWs [2]. The rectifiers used for the conversion from received AC signal to the DC signal need to be designed in such a way to provide adequate power to the implants.

Typical rectifiers using diode bridges have a large forward voltage drop and, hence cannot rectify low-input voltage signals. Though various architectures like synchronous rectifiers [6] and threshold reduction techniques [4] have been proposed to avoid the high forward voltage drop, they need extra circuitry for the cancellation of the threshold voltage. The active components used for threshold cancellation limit the frequency range of operation of the rectifier. This paper presents a voltage doubler based voltage boosting rectifier for a wireless power transfer system applicable to implantable biomedical devices [3].

The paper is organized as follows: Section II of the paper presents the design and working principles of the rectifier. The simulation results are presented in section III, and the concluding remarks are presented in section IV.

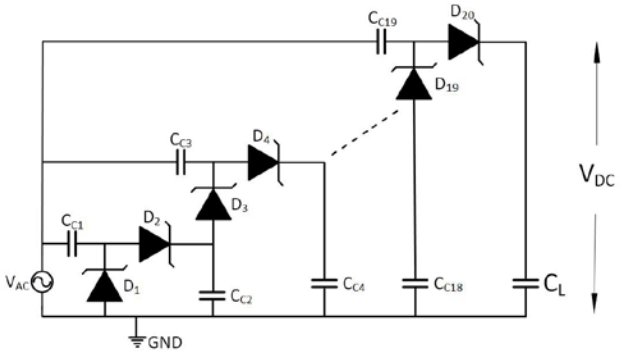

Fig. 1 Schematic of the rectifier circuit.

II. DESIGN ARCHITECTURE

The rectifier presented in this paper is a 10-stage voltage doubling rectifier designed using the Schottky diodes and dual-MIM capacitors (Fig. 1) available in the 130 nm standard BiCMOS process. All the capacitors in the design are chosen to be 1 pF, which is small enough capacitance to provide a higher output voltage and a higher frequency range of operation. A previous version of this rectifier design is presented in [3], which is designed using the 0.5µm process. The previous work provides a brief explanation for choosing 10-stages and also the detailed operation principal of the rectifier. The previous design has been improved by modifying the capacitors in the design to make it work for a wider frequency range. The work presented in this paper utilizes the 130nm BiCMOS process Schottky diodes which have a forward voltage drop of 120 mV, which is lower than that of the 0.5µm Schottky diodes. A lower forward voltage helps the electrons to cross the energy bandgap of the diode at a faster rate, hence improving the switching speed. The capacitors (C_{C1} to C_{C19}) are called the loading capacitors, as they are used to transfer the charge from one stage to the next by holding the charge of one stage during the "charge" cycle and discharging through the next stage during the "discharge" cycle. This results in the multiplication of the voltage through each stage, thereby generating an output voltage of,

$$V_{out} = 10 \times (V_{in} - V_{diode}) \quad (1)$$

Where V_{out} is the output DC voltage at the output node of the 10-stage rectifier, V_{in} is the input AC voltage and V_{diode} is the forward bias voltage of the Schottky diode. For the simulation and characterization of the rectifier, a load capacitor, C_L of 1 pF is used at the output node of the rectifier.

III. Simulation Results

The design is simulated using the Cadence Virtuoso custom IC design tool. A frequency of 7.25 MHz is chosen for the input signal as the rectifier is set to work in a near-field communication environment [3]. From the simulation result it can be seen that a low input AC signal of 100mV and 7.25 MHz is rectified and boosted to a DC voltage of 750 mV by the designed rectifier (Fig. 2). Fig. 2 also shows the increasing output voltage yield and the power conversion efficiency (PCE) for various input voltages. The power conversion efficiency is calculated as

$$PCE = (Po_{ut}/P_{in}) \times 100\% \quad (2)$$

The rectifier is observed to work over a wide range of frequencies. Fig. 3 shows the output DC voltage of the rectifier varying from 10 kHz to 150 MHz frequency range for an input voltage of 200 mV. The output voltage is almost constant (2 V) up to 100 MHz.

The design is compared with contemporary works (Table 1) and the simulation results show better stability for a wider frequency range compared to the other works. Fig. 4 shows the layout of the proposed rectifier design. The layout occupies an area of 102.9 µm × 425.41 µm.

TABLE I. Comparison with other works

	Process	*Input Voltage*	*Output Voltage*	*Frequency of operation*
[1]	130nm	360mV	160mV	NA
[2]	180nm	200mV	1V	10 MHz
[3]	0.5um	200mV	1.5V	10 KHz – 13.56 MHz
[4]	180nm	0.8V	0.6V	40 – 50 MHz
This Work	130nm	200mV	2.03V	10KHz – 100 MHz

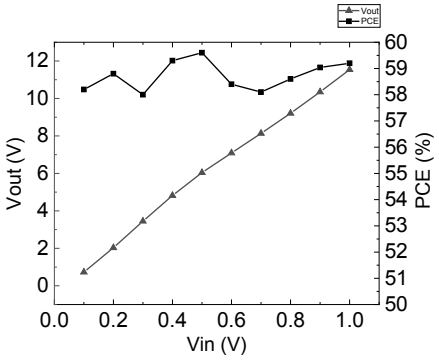

Fig. 2 Output voltage for various input voltages.

IV. Conclusion

A 10-stage voltage boosting rectifier is designed to work for a wide range of frequencies with a power conversion efficiency of 59%. The rectifier is simulated in 130nm BiCMOS process using Schottky barrier diodes and dual-MIM capacitors for a better rectification at lower input voltages. The fabricated chip will be measured and compared with the simulation results for a detailed review of the design's real-time performance in the future.

References

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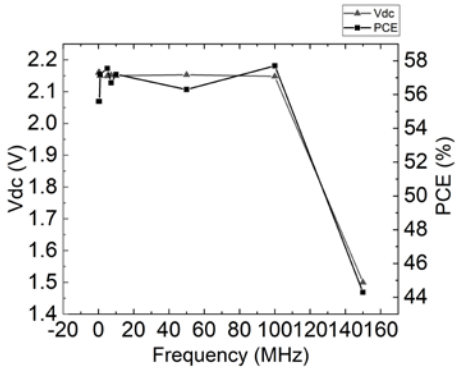

Fig. 3 Output voltage of the rectifier for a wide frequency range of input signal.

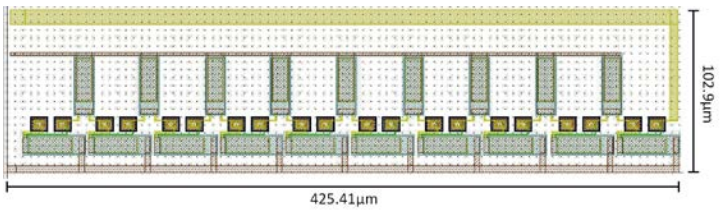

Fig. 4 Layout view of the designed rectifier in 130nm process