Submillimeter-Wave Schottky Diodes based on Heterogeneous Integration of GaAs onto Silicon

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***Abstract*—This paper reports on the design and fabrication of quasi-vertical Schottky diodes for submillimeter-wave applications. Use of the diodes to implement an integrated 160 GHz frequency quadrupler are described.**

I. Introduction

Schottky diodes remain a critical device technology for applications in the submillimeter region of the spectrum (300—3000 GHz). This paper reports on recent work and a new approach to realizing vertically-oriented Schottky diodes that can be readily integrated into planar millimeter and submillimeter-wave circuits [1]. The diode structure is based on heterogeneous integration of the diode epitaxy to a host, high-resistivity silicon substrate that supports both the vertical diode and its associated circuitry. A primary motivation for investigating vertically-oriented diodes is their potential for smaller device parasitics compared to diodes that have coplanar anode and ohmic contacts

II. Quasi-Vertical Schottky Diode

Figure 1 shows a scanning electron micrograph of the quasi-vertical diode reported here. The diode consists of a top-side anode contact, a mesa of GaAs/InGaAs epitaxy, and a bottom-side ohmic contact bonded to a high-resistivity (ρ >10 kΩ-cm) silicon substrate. The structure of the device allows the ohmic contact to be placed in close proximity to the anode and employs an airbridge anode contact to reduce parasitic capacitance.

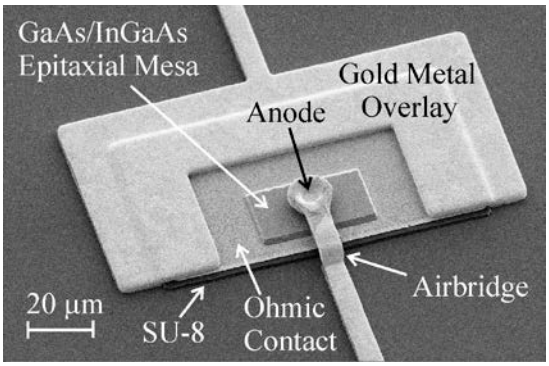

Fig. 1. Scanning electron micrograph of a heterogeneously-integrated quasi-vertical Schottky diode.

III. Diode Fabrication Process

The diode fabrication process utilizes epitaxy consisting of a 650 μm semi-insulating GaAs handle with 1 μm AlGaAs etch stop layer, n-GaAs (280 nm, 2×10^{17}cm^{-3}), and n+-GaAs (1 μm, 5×10^{18} cm^{-3}) device layers [2]. In addition, a 50 nm highly doped (>10^{19} cm^{-3}) InGaAs cap layer is included in the epitaxy to allow the formation of a low resistance ohmic contact using a Ti/Pd/Au/Ti metal stack-up that does not require annealing.

The process to fabricate the diode consists of initially forming an ohmic contact on highly-doped GaAs. This step is followed by a transfer of the epitaxy whereby the ohmic metal contact is bonded to a host silicon substrate using SU-8 (~250 nm thick) as an adhesive. The low curing temperature of SU-8 (100–140ºC) coupled with its relatively lower percent volume shrinkage after cross-linking results in a robust epitaxy transfer that eliminates cracking or delamination. Subsequently, most of the GaAs is removed through wet chemical etching, leaving mesas upon which the diodes are formed using standard photolithographic processes.

IV. Diode Characterization

A Keithley 236 source measurement unit was used for dc characterization of the quasi-vertical diodes. Fitting of the measured current-voltage characteristic provides estimates of the reverse saturation current, ideality factor and series resistance, provided in table 1. The silicon substrate contributes a leakage resistance of ~230 kΩ, which is noticeable in the dc current-voltage characteristic, but is inconsequential compared to the typical diode impedance at submillimeter-wave frequencies. The series resistance and ideality factor extracted from the dc measurements are comparable to those achieved with previous quasi-vertical diodes that utilized annealed contacts.

TABLE I

Diode DC Parameters and Parameters Normalized to Anode Area

Ideality factor	Resistance	Saturation current	Normalized Conductance	Normalized Saturation Current
1.19	4.2 Ω	0.1 pA	33.7 mS/μm^2	0.014 pA/μm^2

High frequency characterization of the diodes was performed in the WR-2.2 (325—500 GHz) band using an Agilent PNAX network analyzer and Cascade Microtech PA200 probe station equipped with WM-570 frequency extenders from Virginia Diodes, Inc. and WR-2.2 on-wafer probes manufactured by Dominion MicroProbes, Inc. An on-wafer calibration was performed using standards fabricated on the same substrate as the diodes. Fig. 2a shows on-wafer measurements comparing quasi-vertical diodes employing both non-alloyed Ti/Pd and annealed Au/Ge ohmic contacts. The measured reflection coefficient (S_{11}) data is shown at midband (425 GHz) as a function of bias voltage. The difference in sweep range vs. bias between the two sets of data is due to a difference in the measurement reference plane for the two diodes. The diode junction capacitance and series resistance, extraxted from the S-parameter data, are shown in figs. 2b and 2c. The extracted junction capacitance for the annealed and unannealed diodes are, as anticipated, the same. The zero bias junction capacitance normalized to anode area is 1.78 fF/μm^2. The series resistance extracted from these measurements indicate approximately 1 Ω lower value for the Ti/Pd ohmic contact compared to the annealed Au/Ge ohmic contact.

V. Application – Frequency Multipliers

The quasi-vertical diodes described above have been applied to implement a fully-integrated frequency quadrupler operating at 160 GHz [3]. The layout of the chip for the balanced quadrupler is shown in fig. 3(a). Two inputs are fed to a pair of balanced doublers with quadrature (0/90º) phase. The outputs of these doublers are of equal amplitude and out-of-phase. Consequently, they can directly drive an output balanced doubler stage, thus producing a frequency quadrupler.

The diodes comprising the circuit are fabricated as described above. Once fabrication of the diodes is completed, the silicon carrier to which they are bonded is thinned and micromachined to form an integrated chip with geometry tailored to fit the waveguide housing to which it will be affixed. An SEM of the multiplier chip is shown in fig. 3b.

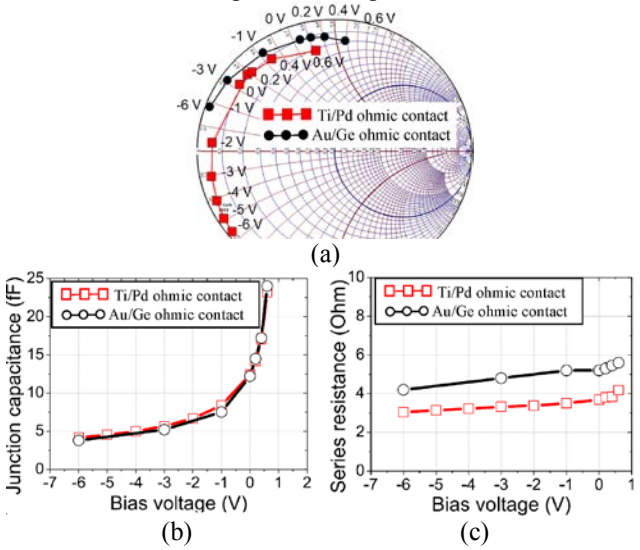

Fig. 2. On wafer measurement results. (a) S_{11} vs voltage at 425 GHz. (b) Junction capacitance, and (c) diode series resistance.

Characterization of the quadrupler is done using an Agilent E8257D frequency synthesizer followed by a Spacek Labs SP408-35-26 amplifier with 35 dB gain and 36 to 43 GHz bandwidth. An Erickson PM5 power meter is used to measure the multiplier output power in the WR-5.1 band. Peak efficiency of 25.5% occurs for an input of 280 mW and bias of -12 V. A maximum output power of 100 mW (20 dBm) was achieved at 159 GHz. This maximum output power corresponds to an input available power of 650 mW and overall quadrupler efficiency of 15% under these operating conditions.

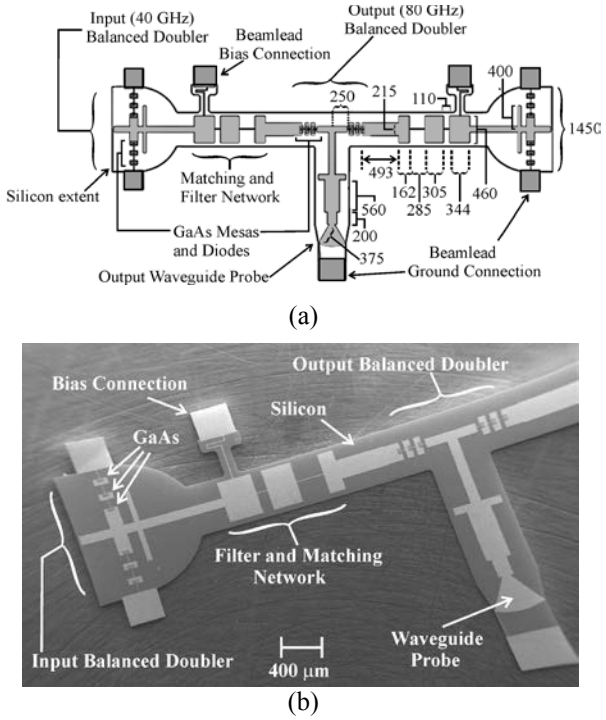

Fig. 3. (a) Quadrupler circuit architecture. (b) SEM image of the completed quadrupler chip.

Acknowledgement

This work was supported by the National Ground Intelligence Center under contract W911W5-16-C-0007 and the National Science Foundation under grant ECCS 1731635.

References

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