Towards Multiplierless Digital Architectures for Aperture Arrays with 1024 RF Beams: A 32-Beam Building Block at 5.8 GHz

Arjuna Madanayake⁽¹⁾, Renato J. Cintra^(2,6), Soumyajit Mandal⁽³⁾, Viduneth Ariyarathna^{*(1)}, Sravan Pulipati⁽⁴⁾, Suresh Madishetty⁽⁴⁾, Diego Coelho⁽⁵⁾, Leonid Belostotski⁽⁶⁾, and Ted Rappaport⁽⁷⁾

(1) Florida International University, Miami, FL, USA
(2) Universidade Federal de Pernambuco, Recife, Brazil
(3) Case Western Reserve University, Cleveland, OH, USA
(4) University of Akron, Akron, OH, USA
(5) Independent Researcher, Calgary, AB, Canada
(6) University of Calgary, Calgary, AB, Canada
(7) New York University (NYU), Brooklyn, NY, USA

Aperture arrays with a large number of simultaneous, sharp, and broadband radiofrequency (RF) beams are becoming important in multiple areas, including wireless communications, radar, and imaging. Fully-digital multi-beam beamformers are expensive in terms of both computational (circuit) complexity and power consumption because of the need for a dedicated RF front-end and data converter for each antenna element in the aperture. The digital signal processing (DSP) required for forming multiple RF beams in real-time further increases the computational complexity and power consumption. The two-dimensional (2D) discrete Fourier transform (DFT) is commonly used to generate orthogonal far-field beams from 2D antenna arrays. For example, the matrix of measurements from an *N*-by-*N* square antenna array aperture can be Fourier transformed to generate N^2 orthogonal beams. Fast Fourier transforms (FFTs) allow the DFT to be computed in an efficient way, i.e., using only $O(N \log N)$ multiplicative operations. Nevertheless, for large N, parallelized FFT cores still account for most of the chip area and power consumption of a fully-digital multi-beam beamformer. In this talk, we use approximate computing to further reduce these area and power requirements. We propose DFT-like transforms that have a *multiplicative complexity of zero* at a cost of only ~2 dB penalty in the worst-case side-lobe level. By trading side-lobe performance for lower area and power, such approximate DFTs allow considerable savings in the overall size, weight, and power consumption (SWaP) of massively multi-beam digital beamformers. We have validated the proposed approach on a fully-functional 32-element receiver array that operates at 5.8 GHz. The design uses 32 parallel ADCs for sampling the antenna outputs and a multiplierless low-complexity DFT approximation (implemented on a Xilinx FPGA on a ROACH-2 platform) for computing 32 RF beams in real-time. The measured RF beams show a per-beam bandwidth of >120 MHz when all 32 beams are realized in real time, with only marginal (≤ 2 dB) degradation in beam performance compared to a control experiment based on a Cooley-Tukey FFT core. The proposed 32-beam implementation is designed as a sub-system for a 1024-beam aperture array that completely eliminates digital multiplications by using parallelized 32-point approximate DFTs.