MICS Band Digital Voltage-Controlled Oscillator (DVCO) for Low-Power Biomedical Data Transmission

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Abstract—**In a typical wireless transmission of medical data from implantable sensors devices Medical Implant Communication System (MICS) protocol with low-power, short-range (~2 m), high-data-rate, 401–406 MHz communication network scheme is employed. This paper presents a digital voltage-controlled oscillator (DVCO) featuring low-power consumption, wide tuning range, and low phase noise suitable for use in wireless transmission of biomedical data employing MICS protocol. The circuit is realized in a 0.13-µm standard CMOS process and consumes less than 600-µW of power, achieves more than 15-MHz/V of analog tuning gain, 370-mV of voltage swing and -106 dBc/Hz of phase noise. Simulation and measurement results demonstrate potential application of the circuit in biomedical sensors system.**

I. INTRODUCTION

In order to precisely measure the physiological parameters such as blood glucose level, various types of implantable sensors have been proposed [1]-[3]. Haider *et al.* have proposed a frequency-shift keying (FSK) scheme for both data and power transmission to achieve better noise immunity while avoiding any power amplifier nonlinearity issues [4]. The FSK carrier frequency can be achieved by a digital voltage-controlled oscillator (DVCO) featuring low-power consumption, wide tuning range and low phase noise. The DVCO may be modulated by FSK signal directly and transmit in a clean band. This paper presents design of a DVCO that can achieve these performance criteria in an implanted sensor system and realized in a standard CMOS process employing MICS protocol. Federal Communication Commission (FCC) has opened 10-channel 402-405 MHz band with 300 kHz each for Medical Implant Communication Service (MICS) unlicensed personal use [5]. Commercial MICS band transceiver features about 10 mW of power consumption, minimum of four external components for implant configuration, high data rate (maximum 800 kbps), low bit error rate (BER) and is packaged in 48 pin Quad Flat No-leads (QFN) package [6].

II. DESIGN OF THE DIGITAL VOLTAGE-CONTROLLED OSCILLATOR (DVCO)

The schematic of the proposed DVCO structure is shown in Fig. 1. The DVCO is basically a cross-coupled LC structure with complementary PMOS and NMOS pairs. DC current is biased with PMOS current mirror for lower flicker noise, which will be mixed up to in-band frequency that is further translated to the phase noise. C_{b1} and C_{b2} are 2-bit capacitor banks that handle differential FSK signals. C_{c1} and C_{c2} are 3-bit capacitor banks that coarse tune center oscillation frequency, which is further fine-tuned by V_{tune} upon varactors, C_{f1} and C_{f2}. Desired oscillations are obtained at differential nodes, V_{op} and V_{on}.

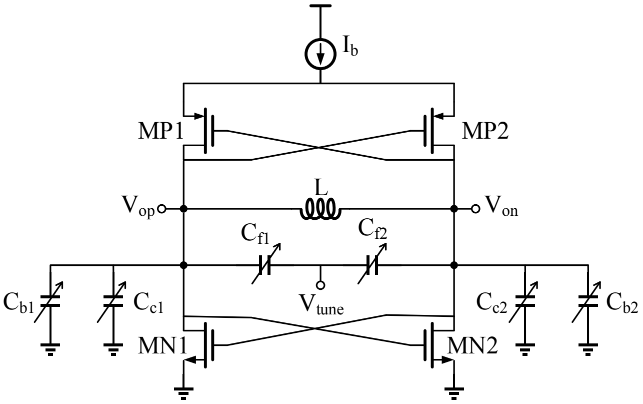


Fig. 1: Schematic of the proposed digital/voltage-controlled oscillator (DVCO).

III. SIMULATION AND MEASUREMENT RESULT

The designed oscillator has been simulated using Cadence^{TM} design tools in terms of transient and frequency response and phase noise. The fabricated CMOS IC has also been tested in order to compare with the simulation results with experimental data. Fig. 2 shows the simulated and the measured transient responses of the oscillator. The resulting frequency spectrum with a center frequency at about 405 MHz is shown in Fig. 3. Phase noise simulation of the proposed MICS oscillator was performed with harmonic balance noise analysis. The phase noise is found to be -106 dBc/Hz at 100 kHz offset and -127 dBc/Hz at 1 MHz offset as illustrated in Fig. 4.

The proposed MICS consumes less than 600-µW power, achieves more than 15-MHz/V analog tuning gain, 370-mV voltage swing and -106 dBc/Hz phase noise. Table 1 presents a summary of the performance comparison of VCOs found in literature with DVCO of this work. The figure of merit (FoM) of the design can be calculated by,

$$FOM = -10\log\left(\frac{kT}{P}\cdot\left(\frac{f_{o,max}-f_{omin}}{\Delta f}\right)^2\right) - \mathcal{L}\{\Delta f\} \tag{1}$$

where, f_o is the carrier frequency, Δf is the frequency offset, P is the power consumption and $\mathcal{L}\{\Delta f\}$ is the phase noise measured at an offset Δf from the carrier. From (1) the figure of merit is obtained to be -156 for the designed DVCO. The comparison result is shown in Table 1, which indicates that for same technology, proposed design consumes less power and achieves better figure of merit.

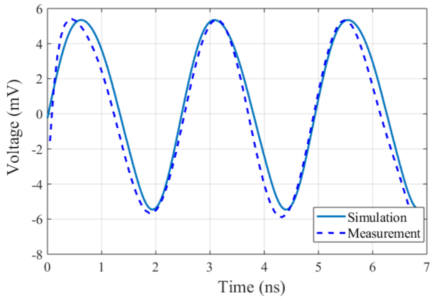
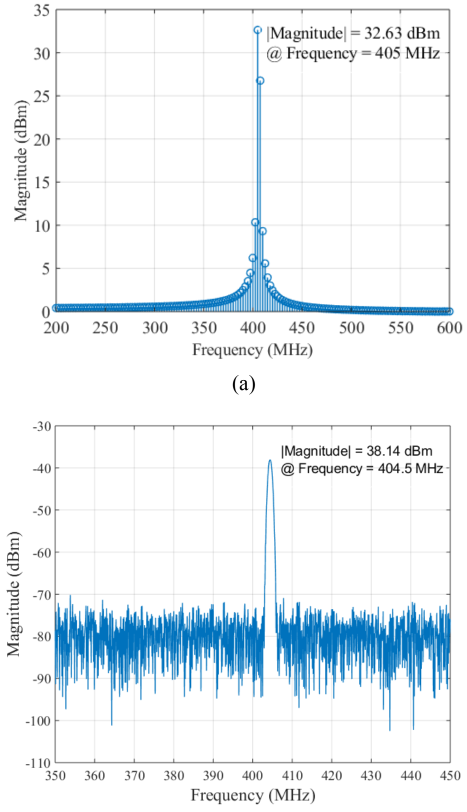


Fig. 2. Transient response of the oscillation with a center frequency of 405 MHz and peak-to-peak voltage swing of 13.8 mV.



(a)

(b)

Fig. 3: Frequency spectrum of the DVCO. (a) Simulation result and (b) measurement result.

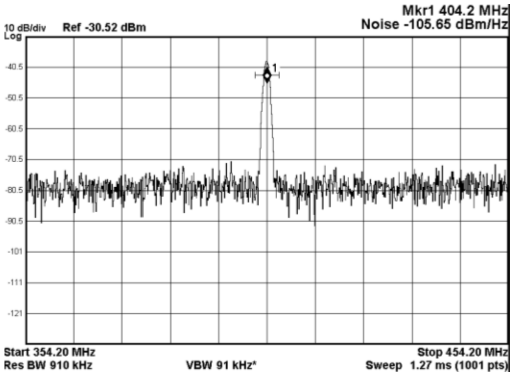


Fig. 4: Measured phase noise of the oscillator. Phase noise is about 106 dBc/Hz at the frequency 405 MHz.

TABLE 1. PERFORMANCE COMPARISON OF THE DESIGNED DVCO

Ref.	Tech. (µm)	Freq. (MHz)	Phase Noise (dBc/Hz)	Power (mW)	FoM (dBc/Hz)
[7]	0.18	400	-93.5@ 0.16MHz	1.05	-161
[8]	0.18	400	-110@ 1MHz	2.0	-179
[9]	0.13	400	-123@ 0.1MHz	1.2	-194
[10]	0.13	402	-127@ 1MHz	1.0	-179
[11]	0.18	402	-140@ 1MHz	3.1	-207
This work	0.13	405	-106 @ 0.1MHz	0.6	-156

IV. CONCLUSION

This paper presents a design of a DVCO structure which has been implemented using a 0.13-µm standard CMOS process. The proposed design has achieved better performance in terms of power consumption, tuning gain, and phase noise. The simulation and the measurement results demonstrate performance figures suitable for potential application in low-power biomedical sensors system such as implantable sensor for monitoring of blood glucose level, lactate in bloodstream, pH or oxygen in a physiological system/environment.

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