Analog Coprocessors for Solving Partial Differential Equations

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Almost all natural systems that are described by classical physics are modeled using partial differential equations (PDEs). The solutions to PDEs represent continuous-valued (analog) physical quantities, such as temperature, pressure, electromagnetic fields, voltage, and current, that change continuously with time. In general, PDE-based systems are solved using fully-discrete numerical methods (discretized both in space and time) such that they can be evaluated using digital computers. However, since physical systems are time-continuous, it is more natural to solve them using analog computing systems that also keep the time dimension continuous. Furthermore, since digital systems are approaching clock speed and transistor density limits, it is unlikely that the computation speeds can continue to improve exponentially using only traditional digital approaches. Our objective is to design a power efficient analog-digital hybrid computation platform that overcomes the speed limitations of existing digital computers to solve a range of linear and non-linear PDE-based simulation problems. The proposed approach allows us to trade-off the accuracy of the solution in return for potentially drastic improvements in the computation speed of selected problems.

Two analog computing algorithms and circuit architectures are developed to compute the continuous-time solution of PDE systems. In the first method, which is limited to linear PDEs, the partial derivatives operating on the spatial dimensions are approximated using discrete finite differences. The resulting spatially-discrete time-continuous transfer functions are used to design analog modules that compute the solution. Specifically, the modules are interconnected in a systolic array architecture to compute the solution over the spatial grid. The second method, which is aimed at electromagnetics problems, replaces the discrete time difference operators in the standard finite-difference time domain cell (Yee cell), using a continuous-time delay operator that can be realized as an analog all-pass filter (APF). The summing and scaling operations in the Yee cell are realized using operational amplifiers. Both solvers were first realized using ideal analog circuits and simulated for different boundary conditions in Cadence Spectre. The wave equation solver was implemented in an analog CMOS integrated circuit. Specifically, a 16-spatial point 1-D version (i.e., using 16 analog modules) for solving simple electromagnetic problems was designed in 180 nm CMOS technology.