A Flexible FPGA Development Environment for the SWOT On-Board Radar Processor

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The Surface Water and Ocean Topography (SWOT) mission's primary instrument is a Ka-band Radar Interferometer (KaRIN). With a sophisticated FPGA-based onboard processing system, the KaRIN instrument is one of the most complex imaging radars JPL/NASA has flown. Traditionally with systems containing multiple FPGAs, each device is developed in near isolation by a cognizant developer. As the design of each FPGA matures, the hardware blocks are merged for system-level lab-based integration. This common approach to FPGA design has proven inadequate for the complexities of the SWOT on-board processor which comprises five interdependent FPGAs performing many real-time signal processing tasks. The need for more comprehensive configuration control, more efficient developer collaboration capabilities and deeper design visibility across the project level has exposed shortcomings in the traditional design approach, and spurred the creation of a flexible development environment geared towards highly collaborative, large-scale FPGA deployment. We expect adoption of our FPGA development environment for both current and future JPL/NASA missions.

The JPL-Tool Configuration System (JPL-TCS) was developed to enable collaboration, consistency with design hand-off capabilities, and visibility into complex FPGA design tasks spanning multiple developers, devices and projects. FPGA design and implementation tools have a well-earned reputation for notorious levels of difficulty and obscurity. Indeed, even the most seasoned digital design engineers continue to fight hard-won battles with the various HDL synthesis, simulation and physical implementation tools. JPL's approach to modernizing FPGA design involves improving portability, cross-platform and implementation repeatability, tight version control, greatly improved collaboration capabilities and code reuse. With JPL-TCS, we have intentionally minimized process control to maintain the developer's creative initiative, while enabling an efficient collaboration infrastructure. This talk will focus on our design philosophy and environment for creating modern, complex FPGA-based radar processors.