**Investigation of Lateral Space Wave and Surface Wave on the Link Budget of Chip-to-Chip Switched-Beam 60-GHz Array**

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Millimeter-wave wireless links can provide high bandwidth, directional gain and throughput with proper design of antennas in Multicore Multichip (MCMC) computing architectures (Melde et. al. *IEEE Trans. Compon. Packag. Manuf. Technol.,* Nov. 2013). Fig. 1 shows antenna arrays (routers) on multicore chips that serve to route data from one chip to another. Antenna arrays for MCMC architecture have a unique pattern reconfiguration requirement of azimuth (lateral) scanning of main beam for interchip wireless communication. This requirement is quite different from pattern reconfiguration in WLAN and WiFi links, in which beam formation is mostly broadside. The lateral direction of beam scanning in MCMC means that the nature of wave propagation along air-dielectric interface of the antenna substrate can play a critical role in determining the link budget, and ultimately the network and computing performance.

This paper will present a wireless link model between 60-GHz circular patch arrays for MCMC architecture, addressing the air-dielectric wave propagation phenomenon. The model is an extension of Friis Transmission equation, taking into account lateral space and surface wave effects. Full wave simulation of 60-GHz antenna arrays separated by some far-field distance will be performed and compared to the analytical model to determine the model's accuracy. Although the excitation of lateral space and surface waves is considered undesirable in some antenna applications, this is not likely to be the case for far-field chip-to-chip communication in which the antenna main beam is desired to be in lateral direction. The link model will be developed for thin substrates considering decay characteristics of lateral and surface waves at typical chip-to-chip separation distances. The model will enable optimization of network topology such as placement of chips in MCMC architecture for efficient and interference free communication.

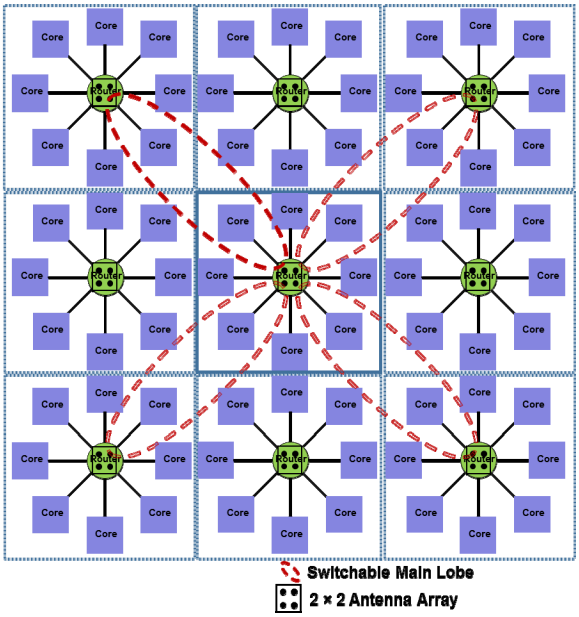


Fig. 1. MCMC architecture showing 3 × 3 arrangement of chips with eight cores per chip