A Low-Power Impulse Radio Ultra-Wideband (IR-UWB) Transmitter for Biomedical Sensor Applications

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***Abstract*— In this paper an UWB impulse radio transmitter for a low-power wearable respiration monitoring sensor is proposed. The transmitter operates in the 3.1 to 5 GHz oscillation frequency range with a tunable channel bandwidth of 0.8 – 1.3 GHz. Implemented in a standard 130-nm CMOS process the proposed transmitter follows on-off keying (OOK) modulation scheme and consumes an average power of 8.2 µW with 1.2 V supply voltage. With a data rate of 1 Mbps, the entire system consumes only 82pJ/bit, which makes it suitable for short distance biomedical sensor applications. Simulation results show that the pulse duration and the amplitude of the impulse signal are 1ns and 0.9 V_{pp}, respectively, with a peak emission power spectrum density of -41 dBm/MHz, which fully complies with the FCC spectral mask.**

I. INTRODUCTION

RFID (radio-frequency identification) tags for vital sign monitoring play an important role for the advancement of *Internet of Things* (IoT). Most of these sensors are powered by harvested energy from different sources such as RF, vibration, heat etc. Because of the power constraint for the energy harvested wireless sensor nodes (100µW/cm^2), ultra-low power design of the readout circuitry along with the transmitter is essential. The traditional narrow band transceivers are not suitable for these applications as they require power hungry PLL (Phase Locked Loop) and PA (Power Amplifier). The pulse based nature of impulse-radio ultra-wideband (IR-UWB) transmitter on the other hand reduces the average power consumption significantly by enabling extreme duty cycling [1]. By minimizing the pulse width of the impulse signal energy consumption can be reduced drastically. In 2002 Federal Communication Commission (FCC) authorized the unlicensed use of the devices in the 3.1 to 10.6 GHz frequency band, provided that the maximum emission power spectral density (PSD) does not exceed -41.3 dBm/MHz or 75 nW/MHz. As the shape and the time duration of the impulse determine the emission power, spectrum and the center frequency, both of them need to be controlled separately so that the emission spectrum follows the FCC spectrum mask regulation. In this paper, a low power on-off keying (OOK) based IR-UWB transmitter fabricated in 130nm process is presented which incorporates precise pulse width control and pulse shaping by modulating a cross-coupled LC oscillator. Triple-well NMOS transistors are used for the oscillator and the buffer circuit to isolate noise and to lower the power consumption by enabling body bias control [2]. This paper is organized as follows: Section II describes the overall CMOS implementation of the proposed the IR-UWB transmitter architecture and the simulation results and is followed by a conclusion in Section III.

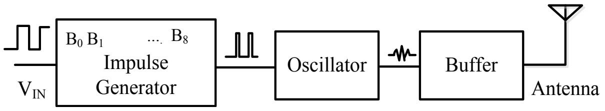

Figure 1: System level block diagram of the UWB transmitter.

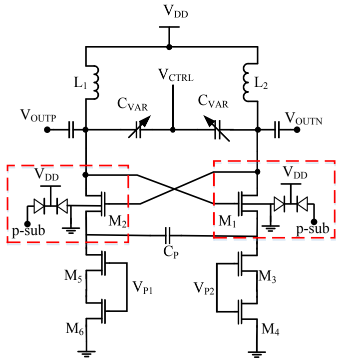

Fig. 2: Tunable cross-coupled differential LC oscillator circuit.

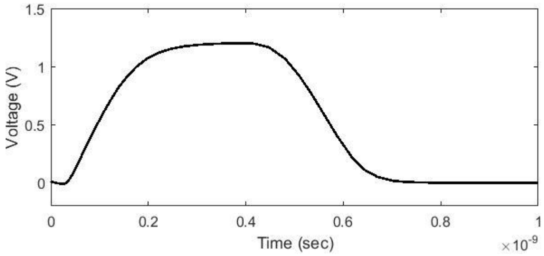

Fig. 3: Post-layout simulation of the impulse signal generated by impulse generator.

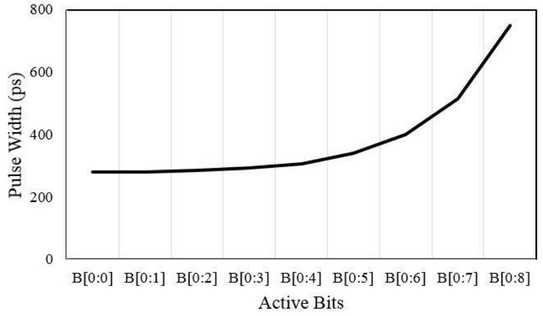

Fig. 4: Pulse width variation of the impulse signal generated by the impulse generator for different bit combination.

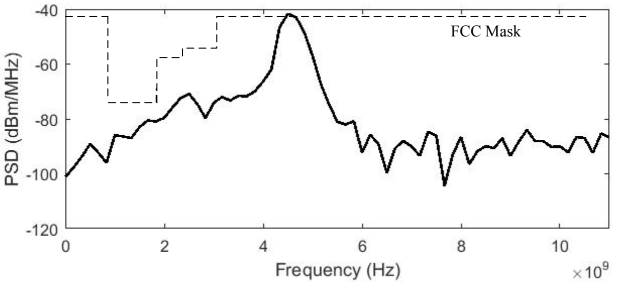

Fig. 5: Power Spectral Density (PSD) of the impulse signal centered at 4.5 GHz frequency.

II. IR-UWB TRANSMITTER ARCHITECTURE

The proposed transmitter, whose block diagram is shown in Fig. 1 has an impulse generator that has 9-bit control signal for achieving tunable pulse width. Since the pulse width, $T_{PW} = \frac{\mathbf{2}}{\boldsymbol{B}}$, the emission power can be controlled by changing the pulse width of the impulse signal the peak. The next block is a tunable cross-coupled LC oscillator followed by a buffer. The transmitter follows on-off keying (OOK) modulation scheme in which binary "1" is represented by a short pulse and binary "0" is represented by no pulse transmission. The core building block of the impulse generator is a tunable capacitor bank, an inverter, a NAND gate followed by another inverter to generate the desired impulse signal. The pulse width of the generated impulse signal is controlled by turning on/off the capacitors in the capacitor bank. The generated impulse signal (V_{p1}) is then delayed by 100 ps using an inverter delay chain. The impulse signals, V_{p1} and V_{p2} are required for the fast startup of the LC oscillator circuit. The LC voltage controlled oscillator (VCO) core consists of the cross-coupled triple-well NMOS FETs (M_{1-2}) and LC tank with inductors (L_{1-2}) and variable capacitors (C_{var}) as shown in Fig. 2. The *p*-well of the triple-well NMOS transistor is embedded within a deep *n*-well creating an isolated body for the NMOS from the *p*-substrate. The center frequency of oscillation can be tuned by changing the control voltage, V_{CTRL}. The impulse signals, V_{p1} and V_{p2} which are generated by the impulse generator block control the turn on and off of the VCO through the tail transistors $M_{3\text{-}6}$. The main aim of this design is to minimize the ON time of the VCO by enabling fast startup and turn off of the VCO instantly. The tail current source of the LC oscillator has been modified to provide asymmetric drive to setup a large initial condition for oscillation, which results in a start-up time of less than 1 ns [3]. The asymmetry in current produces a large voltage difference across the capacitor C_p (=1.56 pF), which enables the fast startup of the VCO. During the ON state the oscillator consumes 5 mA of current, which results in an energy dissipation of ~14.5 pJ/bit for a 3ns pulse. A differential buffer is cascaded after the LC VCO to isolate the oscillator from the load impedance variation. A cascoded class-A topology is chosen for the buffer stage with proper sizing of the M_4 transistor [4]. The high pass filter at the input of the buffer provides good AC coupling to the LC oscillator at the oscillation frequency. The current consumption of the buffer is 8.4 mA during the ON state, which results in 30pJ/bit power consumption with 1.2 V supply voltage.

Fig. 3 shows the post-layout simulation of the impulse signal generated by the impulse generator when all of the digital input bits are set to high. The pulse amplitude is 1.2 V and with a pulse width of 770 ps. Fig. 4 shows the variation in pulse width for different active bits for the impulse generator. The total pulse width can be tuned from 280 ps to 770 ps which corresponds to a bandwidth tuning of ~1GHz. Fig. 5 shows the power spectral density of the signal at 4.5 GHz oscillation frequency. The peak power is approximately -41 dBm/MHz which follows the FCC regulation. The -10 dB signal bandwidth is approximately 800 MHz. The average power consumption of the total system is 8.2 μW with 1.2 V supply voltage, which results in overall power consumption of 82.3 pJ/bit with 1Mbps data rate. The impulse generator block consumes only 2.9 pJ/bit with an ON state current consumption of 0.8 mA. The total area of the transmitter realized in 130nm CMOS process is 600 μm by 600 μm. The balun for the differential output of the buffer and the antenna is realized off-chip for efficient design of the system.

III. CONCLUSION

In this paper a pulse width control scheme for OOK based IR-UWB transmitter designed to be operated at 3.1 - 5 GHz frequency is presented. The impulse generator provides reconfigurable UWB pulses in time domain, which in turn results in spectral control in frequency domain. Fast startup of the LC oscillator is ensured by modifying the tail current source of the VCO. The implemented transmitter is well suited for low power biomedical sensor applications.

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