A Low-Power CMOS Energy Harvesting Circuit for Wearable Sensors Using Piezoelectric Transducers

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***Abstract*—** In this paper, a low-power CMOS AC-to-DC full-bridge rectifier with a switch for piezoelectric transducers is presented. It consists of two NMOS and two PMOS transistors, which are configured to operate as a full-bridge rectifier along with an Op-Amp-based switch control circuit which is connected to a PMOS transistor of the main full-bridge rectifier. With a load of 45KΩ, the output rectifier voltage is 703mV and the input piezoelectric transducer voltage is 694mV. Simulated V_{OUT} versus V_{IN} conversion ratio is 98.7% with an efficiency of 46%. The circuit has been implemented in a standard 0.13µm CMOS process.

I. INTRODUCTION

Recent advancements in wearable and implantable sensor technologies have revolutionized remote patient monitoring such as telemedicine. The power supply required to operate these sensors can be derived from energy harvesting techniques such as using piezoelectric transducers which convert vibrational motion into electric charge. The charge generated by the piezoelectric transducers need to be converted to useful DC voltage for signal processing electronics.

II. PIEZOELECTRIC DEVICE MODELING AND CIRCUIT DESCRIPTION

A piezoelectric device can be modeled in both mechanical and electrical domains that are coupled together, as shown in Fig. 1 [1-3]. In the mechanical domain, the resistor R_M represents the mechanical damping, the capacitor C_M is the reciprocal mechanical stiffness while the inductor L_M represents the effective mass. In the electrical domain, a piezoelectric transducer can be modeled as a current source, which represents the vibrational excitation, with parallel components of a parasitic capacitance, C_P, and a resistance, R_P. Typically, R_P is fairly large compared to the impedance of C_P and therefore can be neglected. Due to the presence of a parasitic capacitor, a piezoelectric transducer has to go through charging and discharging processes before it can actually change its polarity from a positive to a negative value or vice versa. The charging and the discharging behavior of a parasitic capacitor not only results in wasting of the charges of a piezoelectric transducer but also causes a degradation of the efficiency of the rectifier system. In order to recover the charge lost due to the nature of the behavior of a piezoelectric transducer explained above, a switch is deployed at the input of a piezoelectric transducer. The efficiency of the system can be improved further by implementing the control circuits in digital system except the PMOS switch control Op-Amp of the rectifier. The parameter values that have been used for the piezoelectric energy harvesting system are such that, C_P is 25nF, R_P is 1MΩ, I_P is 45µA, C_L is 10µF, and R_L is 45KΩ.

A typical AC-DC full-bridge rectifier consist of four diodes which result in voltage drop due to diode turn-on voltage which is typically 0.5 ~ 0.7V. Fig. 2 shows the circuit diagram of the proposed circuit which provides a lower voltage drop compared to a conventional structure. The output voltage from a piezoelectric device can be calculated using the following equation:

$$V_{RECT} = \frac{I_P}{\omega_P C_P} \quad (1)$$

where, I_P is amplitude of the piezoelectric current and $\omega_P = 2\pi f$, with f being is the excitation frequency of a piezoelectric device, and C_P is a parasitic capacitance of a piezoelectric device. The excitation frequency for the proposed design is 200Hz which provides the theoretical value of V_{RECT} to be 1.43V. However, if a load resistance is considered in the calculations, then the actual output voltage depends on the output load resistance, and can be calculated as follows:

$$V_{RECT} = \frac{R_L I_P}{\sqrt{(1+(2\pi f C_P R_L)^2}} \quad (2)$$

where R_L is 45KΩ in this design. The theoretical value of the output voltage is around 0.92V. However, due to the voltage drop associated with V_{DS} of the PMOS and the NMOS devices, the actual output voltage will be lower than the calculated values. The principle of operation of the piezoelectric device is illustrated in Fig. 3 [4, 5]. As shown in Fig. 3, the charges from a piezoelectric device can be correctly transferred only to the output load after all the charges are transferred to C_P, which lowers the overall efficiency. To save the wasted charges of C_P, a switch in Fig. 2 is used to improve the overall system efficiency. In Fig. 3, the shaded region of I_P waveform represents the lost charge. The mathematical expression for the charge

lost due to the charging and the discharging of C_P can be expressed as follows [5]:

$$Q_{lost/cy} = 2C_P\left(V_{RECT} - (-V_{RECT})\right) = 4C_P V_{RECT} \quad (3)$$

A body biasing circuit is presented in Fig. 4 which prevents any unwanted leakage current. Fig. 5 shows the input amplitude of a piezoelectric transducer. The peak-to-peak amplitude is 1.39V, where the calculated peak-to-peak value is 1.4V. Fig. 6 shows the rectifier output voltage. The amplitude of the output voltage is 0.694V. The simulated conversion ratio of V_{OUT} versus V_{IN} is 98.7% whereas calculated value is 58%. The P_{OUT} of the proposed AC-to DC full wave rectifier is 11.1µW, and the efficiency of the system is 46%. Table 1 shows the summary of the proposed AC-to-DC full-bridge rectifier.

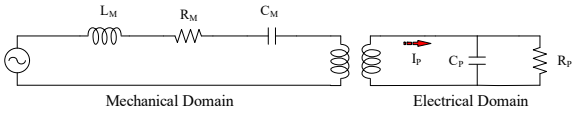

Fig. 1. Scematic of a piezoelectric transducer showing mechnical to electrical domain, [3].

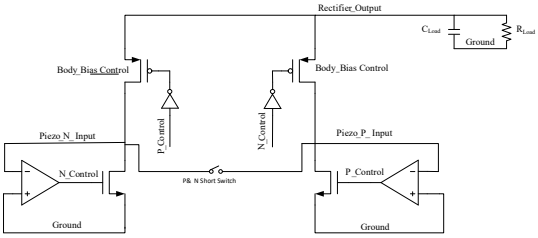

Fig. 2. Proposed AC-to-DC full wave rectifier.

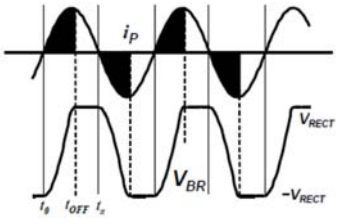

Fig. 3. Voltage and current waveforms for a full-bridge rectifier with a piezoelectric energy harvester [4,5].

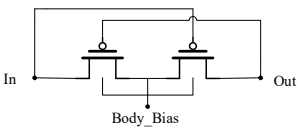

Fig. 4. Body-Bias control circuit.

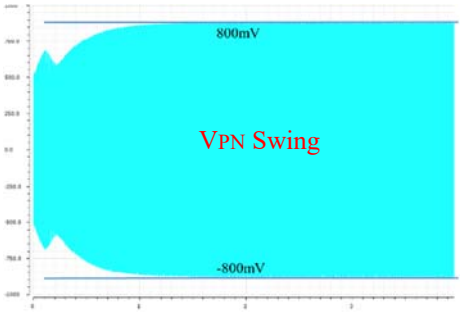

Fig. 5. A piezoelectric transducer output voltage.

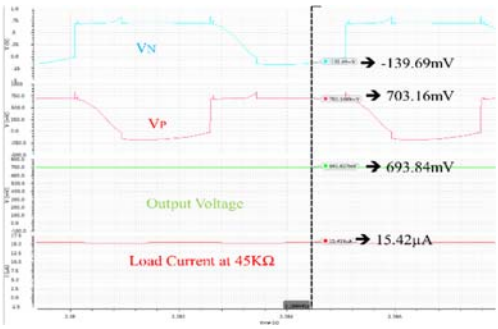

Fig. 6. Rectifier output voltage and load current.

Table 1. Summary of the Proposed Rectifier

Parameters	Simulated
Input Amplitude	0.703 V
V_{OUT}	0.694 V
Frequency	200 Hz
V_{OUT}/V_{IN}	98.7%
P_{OUT}	11.1µW
Efficiency	46%

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