

Phased-Array 64-Element 20-MHz Receiver For Data Capture and Real-Time Beamforming

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Abstract—The Brigham Young University (BYU) Radio Astronomy group, in collaboration with Cornell University, the University of Massachusetts, and the National Radio Astronomy Observatory (NRAO), have developed a phased-array feed receiver with sufficient bandwidth and elements for basic scientific use. This paper summarizes the capabilities of this 20-MHz, 64-element FPGA-based system.

I. INTRODUCTION

Phased-array feeds (PAFs) and their numerous elements require large, complicated receivers. Coupled with the increasing demand for larger bandwidth, PAFs require state-of-the-art hardware and software.

The group at Brigham Young University (BYU) has developed a PAF receiver called the x64 system, which can process 64 antennas across a 20-MHz bandwidth at L-band. In real time the system frequency channelizes received antenna voltages and then (1) streams selected channels to disk, (2) beamforms and power accumulates, and (3) cross-correlates. The system was deployed with a 19-element dual-pol PAF from Cornell University at the Arecibo Observatory in 2013 [1], and is slated for deployment with a 64-element PAF from the University of Massachusetts on the Green Bank Telescope (GBT) later this year.

The aim of this paper is to summarize the operational modes of the x64 system. With its moderate bandwidth, significant number of elements, and real-time processing modes, the x64 system is well-suited for basic scientific surveys, engineering tests, and PAF processing method development. Furthermore, it serves as a springboard for development of a larger bandwidth system that is currently in development.

II. SYSTEM OVERVIEW

The x64 system processing chain receives as input 64 L-band signals that are fed into a 64-input downconverter system [2, 3], which filters, amplifies, and downconverts the L-band signal to a 20-MHz passband centered at 37.5 MHz. These signals are then sampled at 50 MHz by a 64-input, 12-bit analog-to-digital converter (ADC), which causes the passband to alias to a center frequency of 12.5 MHz. These samples are then sent to a field-programmable gate array (FPGA) board named the Reconfigurable Open Architecture Computing Hardware (ROACH) board [4] (shown in Fig. 1). These digitized samples are then frequency channelized and



Fig. 1. The FPGA development board known as ROACH (blue PCB) was used to process PAF data after digitization by the x64 ADC board (green PCB).

either streamed to disk via a 10-GbE link, beamformed and power accumulated, or cross-correlated. We will summarize these three modes of operation in this paper.

A. Data Acquisition System

The data acquisition system (xDAQ) frequency channelizes the received antenna voltages using a polyphase filter bank (PFB) approach for reduced spectral leakage and saves to disk a user-selected subset of frequencies and antennas. When streaming all 64 ADC inputs, the maximum recordable analog bandwidth is 5.76 MHz, which corresponds to 59 raw 16-bit complex (8 bits real, 8 bits imaginary) frequency channels. Fig. 2 depicts a block diagram of the FPGA firmware processing chain.

The data are received by a high-end server PC through a “packet sniffer” software utility. This packet sniffer is custom software called “Gulp,” which is adapted from the multi-threaded code created by Corey Satten at the University of Washington [5].

Under ideal conditions and using a heuristically-sized buffer of 170 GB, the Gulp packet sniffer can acquire on a 3.5-Gbps (≈ 3.41 MHz with 64 antennas and 512-point FFT) data link indefinitely. A bit rate of 5.9 Gbps (≈ 5.76 MHz with 64 inputs and 512-length FFT) is sustainable for nearly ten

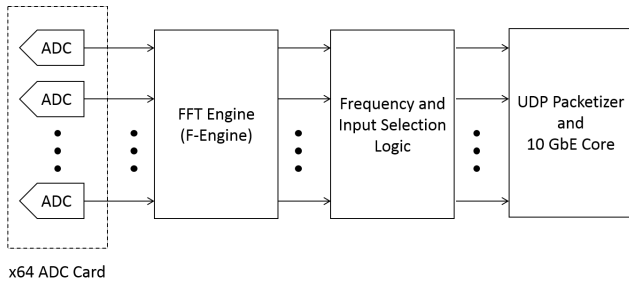


Fig. 2. The data acquisition system frequency channelizes sampled data and packs user-defined frequency channels and feed elements into user-defined protocol (UDP) packets to stream to disk through a 10-GbE connection.

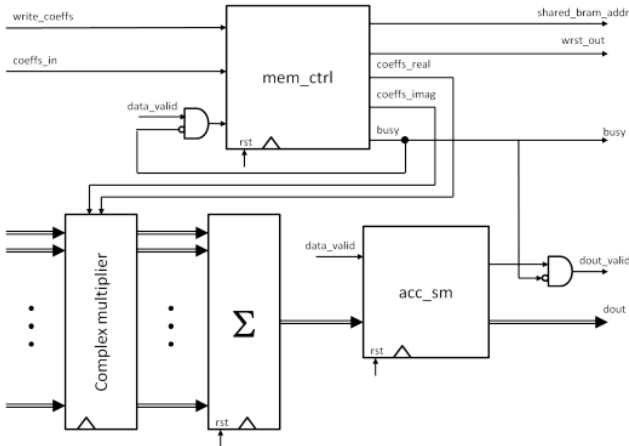


Fig. 3. The xRTB system multiplies beamformer weights contained in BRAM with frequency channelized data and sums to form instantaneous beamformed voltages. These are then power accumulated and saved to shared BRAM.

minutes before buffer overflow occurs. More information about the xDAQ system can be found in [6].

B. Real-Time Beamformer

The real-time beamformer (xRTB) operational mode generates beamformed power-accumulated data for seven simultaneous beams. Each beamformer is fed by 8-bit complex (4 bits real, 4 bits imaginary) frequency channelized data and by 16-bit complex (8 bits real, 8 bits imaginary) beamformer weights that are loaded into local block RAMs (BRAMs) by Python control scripts. A block diagram of a single beamformer for all frequency channels is shown in Fig. 3.

The 32-bit beamformed accumulated powers are saved to shared BRAMs. These BRAMs are then read by Python scripts for a pseudo-real-time display. This operational mode, unlike the data acquisition system, is able to operate on and output the entire 20 MHz bandwidth. Further details about the xRTB mode can be found in [7].

C. Real-Time Correlator

The real-time correlator (xRTC) mode is a derivation of the 32-input correlator designed for the BEST-2 array in Medicina, Italy [8]. The xRTC uses two ROACH boards: the first performs a PFB (2048-point FFT), and the second receives

the channelized data through an XAUI link and correlates. The correlated data are then sent to a server PC through a gigabit Ethernet link and saved as an .hd5 file. More information about this correlator can be found in [8].

III. FUTURE WORK

While this system is capable enough to support simple scientific surveys, there is an ever-increasing demand for larger bandwidths. To this end, a new digital back end is under development for the Focal L-Band Array for the GBT (FLAG) [9]. This new system will support a bandwidth of 150 MHz across 40 elements. It will be able to correlate and beamform this entire bandwidth in real-time using a second-generation ROACH board and graphics processing unit (GPU) cards in order to perform extra-galactic HI and pulsar surveys.

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