

Manufacturable Cryogenic SiGe LNA for Radio Astronomy and Space Communications

Andrew Janzen, Student Member, IEEE, Sander Weinreb, Life Fellow, IEEE

Abstract—This report presents results of recent work on the design of a wideband cryogenic low noise amplifier (LNA). The amplifier operates from 200 MHz to 6 GHz with noise temperatures of 2.8 K and 4.5 K at 1.6 GHz and 5.2 GHz respectively. Design, fabrication and cryogenic test results will be described.

Index Terms—Cryogenic Low Noise Amplifier

I. INTRODUCTION

Designing cryogenic amplifiers has been an active area of research at Caltech for many years. Recent work has focused on the design of a cryogenic low noise amplifier from 1.6 to 5.2 GHz for the Square Kilometer Array (SKA) Wideband Single-Pixel Feed (WBSPF) technology development program. One of the major goals of this research was to design an easily manufacturable, inexpensive, very low noise cryogenic amplifier as the SKA requires hundreds to thousands of amplifiers. These goals have been achieved and this report summarizes the design process and results for a cryogenic SiGe amplifier with 2.8 and 4.5 K noise at 1.6 and 5.2 GHz respectively.

II. UNDERSTANDING SIGE TRANSISTORS

Silicon Germanium (SiGe) cryogenic amplifiers have several advantages compared to traditional cryogenic High Electron Mobility Transistor (HEMT) amplifiers. SiGe is a readily manufacturable process with very good repeatability. Due to their bipolar structure, SiGe devices have better input match at low frequencies and extremely low minimum noise temperatures (~ 1 K), making the technology an excellent choice for cryogenic amplifiers below 8 GHz. For this design the applicable transistors were very high performance (370 GHz F_{max}), silicon germanium (SiGe) bipolar transistors commercially available from ST Microelectronics as the BICMOS055 process [1,2]. The design is thus manufacturable in the sense that all components are commercially available. Fig. 1 shows a Medium Frequency 5GHz (MF5) amplifier using an ST type 055HS transistor as the first stage.

A. Janzen is with the Electrical Engineering Department, California Institute of Technology, Pasadena, CA 91125. (e-mail: ajanzen@caltech.edu)

S. Weinreb is with the Electrical Engineering Department, California Institute of Technology, Pasadena, CA 91125. (e-mail: sweinreb@caltech.edu)

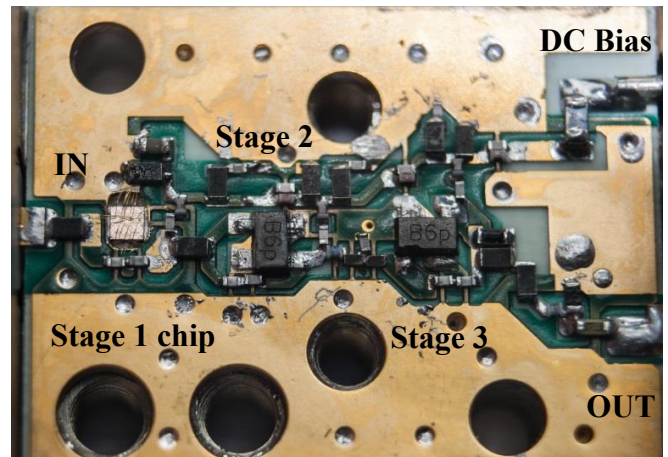


Fig. 1. Layout of an MF5 amplifier used for cryogenic testing. The circuit board is 15.8 x 20.5 mm. An ST Microelectronics chip transistor is used for the first stage while NXP BFU725 packaged transistors are used for stages 2 and 3.

Several MF5 amplifier modules were assembled and tested and these modules provided a testbed to experiment with various transistor sizes. Some of the best results were obtained with the ST 055HS transistors with 4.45 μm effective area which was the largest transistor size in our test reticule. To test the performance of transistors with even larger area, three transistors on the same reticule with effective emitter areas of 4.45, 3.56, and 2.67 μm^2 were placed in parallel giving a total area of 10.7 μm^2 . Increasing the emitter area effectively reduces the R_{opt} impedance which can improve the noise match [3,4]. The transistors were connected using a wire bond stitching technique shown in Fig. 2. Due to the long bond wire lengths associated with stitching the three transistors in parallel, the amplifier oscillated when measured at room temperature but surprisingly was stable when cold.

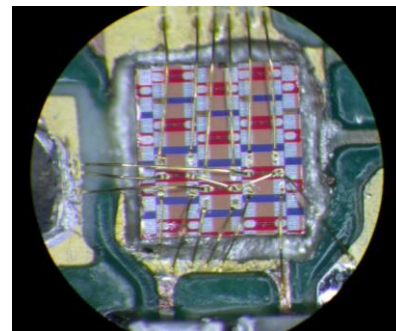


Fig. 2. View of the wirebonding of three parallel ST BiCMOS 055HS transistors inside the MF5 amplifier shown in Fig. 1.

The amplifier was designed as the combination of three cascaded gain stages in series with high pass filter networks to achieve reasonable gain flatness and was based on previous work outlined in [5]. Output attenuation was added to achieve better S22 return loss. Each stage is composed of a common emitter amplifier with a feedback resistor from collector to base to provide bias and improve the input return loss.

III. MEASURED RESULTS

Measured and modeled noise for two MF5 amplifiers is shown in Fig. 3, and cryogenic S parameters for a MF5 amplifier are shown in Fig. 4. Depending on the effective area of the transistor used in the amplifier, the noise match and thus the noise performance will be better at the low or high end of the band. Fig. 3 highlights this, showing measured results which are noise matched at different ends of the band. There are some discrepancies between the measured noise data and the noise model and it is believed this is due to three main factors. First, the noise measurement setup used is only accurate to ± 1 K. Second, the passive components in the circuit may have more complex models than have been used. Third, the model may not account for all of the noise mechanisms in the transistors.

Fig. 4 shows measured and modeled S11, S21, and S22 for a cryogenic amplifier using a single 4.45 μm ST055HS transistor. The model used to design the amplifier accurately predicts these measured responses up to 2.5GHz for S22, up to 5.2 GHz for S11 and up to 10 GHz for S21. The model used did not account for the transistor's parasitic inductances and thus measured results diverge as the frequency increases. The gain differences between the measured data and the model can be reduced by reducing the modeled emitter inductance of the first stage transistor. This alone raised the modeled gain by 5dB across the band. Although most of the components can be accurately modeled before designing the amplifier, the first stage emitter inductance is very difficult to model as a small change in the bond wire length can create a significant change in emitter inductance. As the chip is wire bonded by hand, some variability is inevitable. The emitter inductance plays a key role in achieving noise matching and gain, especially as frequency increases above a few GHz.

REFERENCES

- [1] P. Chevalier, et al. "A 55 nm Triple Gate Oxide 9 Metal Layers SiGe BiCMOS Technology Featuring 320 GHz f_T / 370 GHz f_{MAX} HBT and High-Q Millimeter-Wave Passives." 2014 IEEE International Electron Devices Meeting, 2014.
- [2] P. Chevalier, et al. "Towards THz SiGe HBTs." 2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2011.

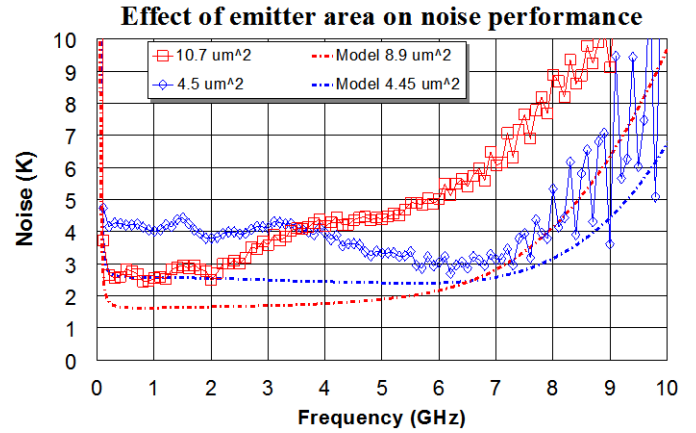


Fig. 3. Modeled and measured noise of two MF5 amplifiers with different first stage emitter areas.

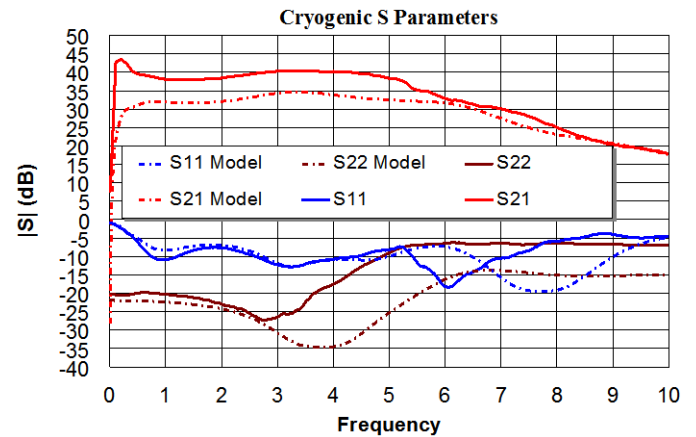


Fig. 4. Measured and modeled cryogenic S parameters S11, S21, and S22 for a MF5 amplifier using a ST055HS transistor with 4.5 μm emitter area.

IV. CONCLUSIONS

This report has presented preliminary measurement results for a manufacturable low noise cryogenic amplifier with applications in radio astronomy, communications, and low temperature physics research. Future work will investigate the design of higher frequency SiGe cryogenic amplifiers, improved noise modeling of the first stage transistor, and optimized narrow band amplifiers for specific applications.

ACKNOWLEDGMENT

The authors would like to acknowledge the collaboration of Pascal Chevalier at STMicroelectronics for providing the test transistors used in this work.

- [3] S. Weinreb, J. Bardin, H. Mani. "Design of Cryogenic SiGe Low-Noise Amplifiers." IEEE Trans. On Microwave Theory and Techniques Vol. 55, No. 11, Nov. 2007.
- [4] J. Bardin. "Silicon-Germanium Heterojunction Bipolar Transistors For Extremely Low-Noise Applications." PhD Thesis, California Institute of Technology, 2009.
- [5] S. Weinreb, J. Bardin, G. Jones. "Matched wideband low-noise amplifiers for radio astronomy." Review of Scientific Instruments, 2009.