Thermo-optically Tunable Linear Photonic Crystal Microcavities in Advanced SOI CMOS Technology

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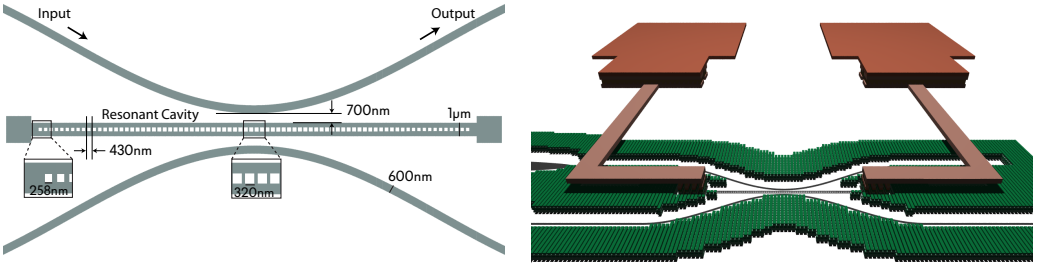
We demonstrate linear photonic crystal (PhC) microcavities with thermo-optic tuning capability realized in the IBM 45 nm (12SOI) silicon-on-insulator CMOS microelectronics fabrication process. The PhC microcavities can be used as efficient integrated optical wavelength add-drop filters. The cavity is created in the monocrystalline silicon transistor body layer of the CMOS process, with a resonance wavelength of 1520 nm. The cavity device layer is doped to lower the electrical resistance so that current sent through it generates local heating with reasonable drive voltages. The dissipated heat increases the temperature of the cavity and, because of the high thermo-optic coefficient of silicon, increases the index of refraction, shifting the resonance wavelength. This method should be more effective than an adjacent metal or polysilicon heater because the hot spot is right in the middle of the optical mode of the cavity.



(a) (b)

Figure 1: (a) Body layer layout of PhC with coupling bus. (b) Full layout of PhC with metal filling and electrical pads.

In the talk, we will present the design considerations for realization of electrically-active PhC cavities. For example, the device body layer in this process has a sub-100 nm thickness which limits optical confinement; and the cavity geometry is constrained by desired electrical properties, optical cavity design constraints, and CMOS process design rules. Cavities are designed by creating a rigorous mapping of mirror strength at a target resonance frequency to a taper parameter, the size of the square holes. This mapping is used to create a linear mirror strength distribution in space and thus a Gaussian electric field envelope. Dopant blocking layers are designed to heavily dope the outer portions of the cavity where the optical field is weak and to lightly dope the center of the cavity where the optical field is strong. This is in order to make sure that the doping does not degrade the cavity optical quality factor (Q), while simultaneously realizing a localized electrical resistor in the cavity. Contact plugs and vias are placed on the edges of the cavity that connect to electrical contact pads on the top of the chip. Fabricated devices and results will be presented.