

NRAO VLBA SYNTHESIZER PROJECT 2013

Steven Durand* ⁽¹⁾, Rob Long ⁽¹⁾, Chip Scott ⁽¹⁾, Jim Jackson ⁽¹⁾, Walter Brisken ⁽¹⁾,
Jon Romney ⁽¹⁾, Craig Walker ⁽¹⁾, and Keith Morris ⁽¹⁾.

(1)- National Radio Astronomy Observatory, PO Box O, Socorro,
New Mexico, USA 87801 - <http://www.NRAO.edu>

The National Radio Astronomy Observatory (NRAO) is developing a new 2-16 GHz synthesizer for integration into the Very Long Baseline Array (VLBA) antennas to support upgrades and enhance performance. The existing VLBA synthesizers have served NRAO well, but are restrictive due to very coarse tuning steps (alternating between 200 MHz and 300 MHz) and limited tuning ability. These synthesizers worked fine with the old narrow bandwidth recording system but are now becoming a hindrance to current and future observing. The new Digital Backend and Mark5C recording capability require new synthesizers to allow full tuning capability and improved performance.

The new NRAO 2-16 GHz synthesizers will offer many advantages over the current design. It will provide flexible tuning, lower phase noise, and generally less maintenance than existing designs. In addition, these new synthesizers are being designed in such a way that functional blocks can be changed to accommodate different frequency ranges (i.e. 2-8 GHz, 8-18 GHz, etc.) without a complete re-design. The heart of the new synthesizer design is a dual, high speed Direct Digital Synthesis (DDS) chip which allows rapid frequency tuning. These features and the innovative tuning scheme allow for exact 10 KHz tuning steps from 2-16 GHz with no gaps. An FPGA is used to interface all monitor and control (M&C) functions between the DDS itself and the Module Interface Board. This feature allows the FPGA to be coded to interface with a variety of M&C systems allowing even greater flexibility. The design uses two YIG oscillators for RF generation and two YIG tracking filters for harmonic rejection. This allows two completely independent RF outputs to be generated with a single module. The YIGs will be phase locked using the available VLBA LO references (100 MHz for the PLL and 500 MHz for the DDS clock) so phase noise will be dictated by the multiplied hydrogen maser noise. Our design goal is less than 200 fs of jitter, or less than 6.2° rms at 86 GHz. Several advantages of the new synthesizer include the ability to access all of the L-band data (1300-1700 MHz) simultaneously and improved RFI avoidance at L, S & C-band.