Overview and Initial Results of a FPGA Based Digital Receiver for Meteor Radar Applications

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In contrast to the fixed signal processing algorithms of conventional analog receivers built using discrete analog components, the signal processing algorithms of digital receivers are implemented in software defined digital logic. Because of software defined signal processing, a digital receiver can process an incoming signal in a virtually limitless variety of ways. A digital receiver is indicated for use in remote sensing applications including unmanned aerial systems (UAS), high bandwidth data acquisition and interfacing to communication systems using complex modulation schemes. Defined by a minimal RF front-end followed by an analog-to-digital converter (ADC) controlled by a reconfigurable logic device (FPGA), the received data is eventually transferred to a host PC for storage and post-processing via a standard communications protocol (in this case USB 2.0). Design and implementation of the current FPGA based digital receiver is discussed. Main hardware components and electrical interfaces are outlined including the Xilinx Virtex 5 FPGA, Analog Devices 9252 ADC, USB interface and USB-based FPGA control and configuration strategy highlighting the end-to-end ADC-to-host PC datapath.

Currently, the digital receiver is configured to facilitate range and radial velocity determination of MLT region meteors for use with the COBRA meteor radar. Methods for determining the optimal sampling and receiver decimation frequencies for aliasing of the radar's RF carrier frequency while maintaining good SNR caused by out-of-band signals are discussed. FPGA based DSP algorithm development and implementation is explored from a system requirements standpoint. Finally, post-processing the received data through IQ demodulation and matched filtering is performed to extract the meteor range and radial velocity parameters from the sub-sampled radar pulses. Initial results from the system will be presented in addition to a system overview.