Scaling Correlator Architectures to Large Arrays of Antennas

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Arrays with hundreds or possibly thousands of reflector antennas, as well as others with millions of wavelength-scale antennas, are now being considered for radio astronomy and to some extent space communications. The problem of scaling cross-correlation architectures for imaging the sky and beamforming to a large amount of antennas is explored in this paper.

As is well known, the computation required to correlate all the baselines for N antennas is proportional to N^2. The large amount of computation required will easily be on the order of 10^{15} operations per second for Gigahertz bandwidth data. This paper will investigate current technologies for performing these computations including Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs) and general-purpose processors. In the past, ASICS were mainly used for state of the art correlators. However, FPGAs have recently begun to rival ASICs in computational power and logic density. In addition, the design cycle is much shorter. General purpose processors have likewise become much more powerful and potentially offer an even greater design cycle advantage. The tradeoffs between these various technologies for new large N correlators will be discussed.

How to deliver the antenna signals to the baseline correlators is a major architecture choice for a large N correlator. While the number of baselines associated with N antennas grows as N^2, the number of logical signal paths between antennas and baselines grows as N^3. Well known constructs such as FFT or polyphase filterbanks and corner turners before correlation move much of the interconnects from wires or cables to silicon level switching. Some chip to chip, board to board or chassis to chassis communication will be needed, however. One major tradeoff for these types of interconnects is whether to go with synchronous or asynchronous communications. Synchronous, clock driven schemes could use parallel high speed wires or generic high speed serial interfaces. Asynchronous high speed serial, packetized data standards such as 10Gig Ethernet, Infiniband, and PCI Express offer a more standardized solution, but some data bandwidth is lost to framing. However, the use of these serial data standards allows the possibility of using commercial packet switches to implement required interconnects. The scalability of these technologies will be explored.