THE IMPACT OF FLIP-CHIP PACKAGING ON RF MONOLITHIC INDUCTORS

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ABSTRACT

Recently, Flip-Chip (FC) package technology has become popular for RF applications. The main reason for that is the shorter interconnects length of the bumps compared to wire bond technology which enhances the interconnect performance at high frequency.

On the other hand, monolithic inductors are important and performance-limiting components in Radio Frequency Integrated Circuits (RFIC's), such as voltage control oscillators (VCO's) and low noise amplifiers (LNA's). The most important parameter of monolithic inductor is its quality factor. Inductor quality factor is limited by the losses. The metal and substrate losses mechanisms have been reported and studied in many literatures. To the best of our knowledge, no literature has reported the effect of package losses on the inductor quality factor.

Although reducing the FC bump height enhances the frequency reponce of the package interconnects, it will results in proximity coupling between the package and upper metal layers of the inductor. This coupling produces additional losses and reduces the quality factor of the inductor.

In this paper, we investigate the effects of the FC packaging on the monolithic inductor quality factor. We evaluate the inductor electrical parameters using full-wave electromagnetic field solver. We present the inductor parameters with and without FC package (see Fig.1). Our investigation helps RF designer to predict accurately inductors parameters including package assembly effects and to reduce redesign cycles.

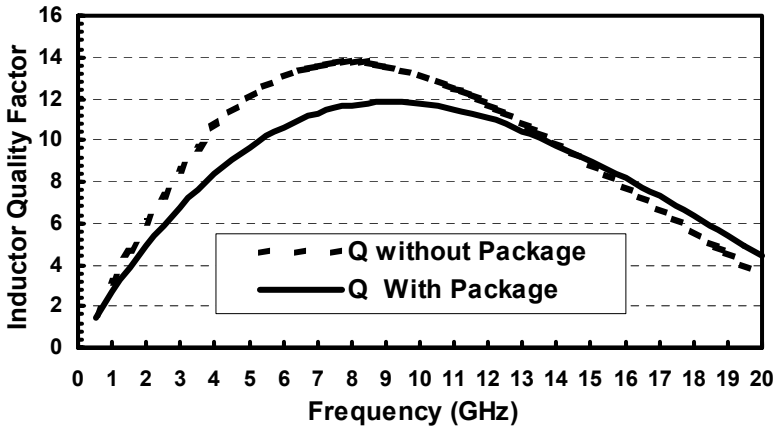

Fig. 1 Example of the package assembly impact on typical inductor quality factor